Bluetooth Baseband LSI

Panasonic PAN1026
Toshiba TC35661

Application Note

August.2013
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<table>
<thead>
<tr>
<th>Date</th>
<th>Modification</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>24th-June-2013</td>
<td>1st Release&lt;br&gt;Based on TC35661_SPP_LE_Application_Note. Added information on the following sections.&lt;br&gt;2.2 Setting up Complete model&lt;br&gt;The part of ATT/GAT on the picture.&lt;br&gt;3. General Supported Function&lt;br&gt;Change three “Supported” to &quot; Under consideration&quot;.&lt;br&gt;4.2.6 Flow chart of initialization&lt;br&gt;In “Flow chart during Complete mode”, add the initial setting for BLE.</td>
<td></td>
</tr>
<tr>
<td>26th-July-2013</td>
<td>2.2 and 3 SPP and GATT connection are exclusive.&lt;br&gt;7.5 TCU_MNG_DEEP_SLEEP_REQ command description.&lt;br&gt;Command description is added.</td>
<td></td>
</tr>
<tr>
<td>6th-August-2013</td>
<td>4.1.3 Communication Timing&lt;br&gt;Interval is changed to 5ms.&lt;br&gt;7.3 External clock setting with LOC_WRITE_MEM command&lt;br&gt;Deleted.</td>
<td></td>
</tr>
<tr>
<td>7th-August-2013</td>
<td>4.2.6 Flow chart of initialization&lt;br&gt;Added the attention words of the HCI_DBUS_WRITE command.&lt;br&gt;8.2 Characteristic improvement&lt;br&gt;New addition.</td>
<td></td>
</tr>
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- **8.2 Characteristic improvement**

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1 TC35661 Complete Model

TC35661 can operate, not only Link Management Protocol but also Stack and Profiles. This system provides with easy development to concentrate the applications for the system. The following shows the difference between general HCI model and TC35661 Complete model.
2 Protocol Layer and Complete model

2.1 Support for Protocol Layer
Following figure shows the supported Bluetooth Protocol and Profile Layer in TC35661.
It is executed RF control, Link Controller, Link Management, HCI, SDP,L2CAP, RFCOMM, SCO,
GAP, SPP Profiles, ATT, GATT and GAP.
The running Bluetooth Protocol / Profile are compliant with the Specification of the Bluetooth
System Version 4.0.

2.2 Setting up Complete model
TC35661 sets HCI mode after to release Reset sequence and is changed to Complete mode by setting
command from Host CPU. The setting value in HCI mode is kept in Complete mode.

SPP and GATT connection are exclusive.
Inquiry/Page scan and LE advertise can be executable at the same time.
When SPP connection is established, GATT connection can not be connected without SPP disconnection.
When GATT connection is established, SPP connection can not be connected without GATT disconnection.
Refer to LE MSC.
## 3 General Supported Function

<table>
<thead>
<tr>
<th>Items</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bluetooth Core</td>
<td>4.0</td>
<td>Legacy(BR)and LE are both supported. HS are not supported.</td>
</tr>
<tr>
<td></td>
<td>Power Class 2</td>
<td></td>
</tr>
<tr>
<td>Feature (Classic)</td>
<td>Sniff</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>Park</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>Hold</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>BR- 5slot packet</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>BR- 3slot packet</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>2M-5slot packet</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>2M-3slot packet</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>3M-5slot packet</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>3M-3slot packet</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>RSSI</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>SecureSimplePairing</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>PowerControl</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>AFH</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>SCO</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>eSCO</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>CQDDR</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>Sniff subrating</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>Secure Simple Pairing</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>UART Baudrate</td>
<td>115.2kbps is default. Selectable by command.</td>
</tr>
<tr>
<td></td>
<td>UART Protocol</td>
<td>H4 (UART Transport Layer).</td>
</tr>
<tr>
<td></td>
<td>Multi Profile/point</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>SPP-A</td>
<td>Supported. Other profile is not supported.</td>
</tr>
<tr>
<td></td>
<td>SPP-B</td>
<td>Supported. Other profile is not supported.</td>
</tr>
<tr>
<td></td>
<td>USB</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>WIFI Co-Ex</td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td>ScatterNet</td>
<td>Not Supported</td>
</tr>
<tr>
<td>Feature (LE)</td>
<td>Central</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>Peripheral</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>Multi Profile/point</td>
<td>Not supported</td>
</tr>
<tr>
<td></td>
<td>ConnectionUpdate</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>Random Address</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>WhiteList</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>SecurityProperty(JustWork)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>SecurityProperty(PassKey)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>SecurityProperty(NumericComparison)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>GATT-Client</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>GATT-Server</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>Broadcaster</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>Oberver</td>
<td>Not supported</td>
</tr>
<tr>
<td>Dual</td>
<td>SPP+GATT connection estblishment simultaneously</td>
<td>Not supported</td>
</tr>
</tbody>
</table>
4 UART Interface

TC35661 has an UART interface to communicate with an external Host CPU. This chapter explains the hardware functionality of UART interface.

4.1 Hardware Functionality

TC35661 UART interface uses 4 signals, TX/RX pins and RTS/CTS pins have the following functions.
1) Programmable baudrate (Default value is 115200bps)
2) Communication with 4 signals (Tx/Rx/RTS/CTS)
3) DataFormat=Start bit+8bit data+1bit Stop bit without parity bit.
4) Support of Error detections, time-out/Over-run/Flaming Error

4.1.1 Formula of Programmable Baudrate

TC35661 UART baudrate can be calculated in the following formula.

\[
BaudRate[\text{bps}] = \frac{\text{InternalBaudrateBaseClockFrequency}}{\text{OverSamplingRatio} \times \text{DividingRatioOfInternalBaudrateBaseClock}}
\]

\(\text{InternalBaudrateBaseClockFrequency}\) is 39MHz. \(\text{OverSamplingRatio}\) is the integral value from 1 to \(2^{16}\). \(\text{DividingRatioOfInternalBaudrateBaseClock}\) is the integral value from 12 to 17, and both can be changed with the UART Sampling Control Register value in M2_BTL_SET_BAUDRATE command.

e.g.)

\[
BaudRate = \frac{39 \times 10^6}{13 \times 26} = 115.4kbps
\]
4.1.2 Communication Timing
The following figure shows the communication timing.

![Communication Timing Diagram]

(Note) Cycle = 7 / setting to baudrate
Tolerance of transfer clock is less than 1.0%.

4.1.3 Error Detection (time-out/Over-run/Flaming Error)
TC35661 UART has error detection function to get more reliable communications.
When TC35661 detects UART communication errors, TC35661 returns HW_Error_Event with error code to inform host CPU of the communication error.
Refer to TC35661_Extention_HCI_Command_XXXX.pdf HW_Error_Event for more detail.
The maximum transmit interval between each byte is 5ms. If this error code occurs, check for the transmission Byte interval from host CPU.
4.2 UART Transport

4.2.1 Packet Format in HCI mode
UART Protocol in HCI mode is based on Bluetooth Core Spec.H4(UART Transport Layer).
The HCI packet indicator shall be sent immediately before the HCI packet.

<table>
<thead>
<tr>
<th>HCI packet type</th>
<th>HCI packet indicator</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCI Command Packet</td>
<td>0x01</td>
</tr>
<tr>
<td>HCI ACL Data Packet</td>
<td>0x02</td>
</tr>
<tr>
<td>HCI Synchronous Data Packet</td>
<td>0x03 (No Support)</td>
</tr>
<tr>
<td>HCI Event Packet</td>
<td>0x04</td>
</tr>
</tbody>
</table>

4.2.2 Packet Format in Complete mode
UART Protocol in Complete mode is based on TOSHIBA original.
The following table shows the packet format of TC35661 UART Transport packet.
The Packet Length shows all length with Interface data and Packet length.
The maximum Packet length is 1019Bytes.

<table>
<thead>
<tr>
<th>Packet Length</th>
<th>Interface Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>3bytes</td>
<td>Nbytes</td>
</tr>
</tbody>
</table>

The following table shows the Interface Data Format. Service ID means Bluetooth Protocol Layer for data field.
OpCode means the content of data field. Length means the volume of data field. The command is input from host CPU to TC35661 and the event is from TC35661 to host CPU

<table>
<thead>
<tr>
<th>Service ID</th>
<th>OpCode</th>
<th>Length</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Byte</td>
<td>1 Byte</td>
<td>2 Bytes</td>
<td>N Bytes</td>
</tr>
</tbody>
</table>

The following table shows the type of Service IDs

<table>
<thead>
<tr>
<th>Service ID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE1</td>
<td>Bluetooth Management Interface</td>
</tr>
<tr>
<td>0xE5</td>
<td>SPP</td>
</tr>
<tr>
<td>0xD1</td>
<td>BLE MNG</td>
</tr>
<tr>
<td>0xD2</td>
<td>BLE GATT</td>
</tr>
<tr>
<td>0xD3</td>
<td>BLE SMP</td>
</tr>
<tr>
<td>Other</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
4.2.3 RTS/CTS Flow Control

This chapter explains the functionality of CTS(Clear to Send)/RTS(Request to Send) signals in UART. CTS signal is used in GPIO9, and RTS signal is in GPIO8. CTS/RTS signals are used to get more reliable serial communication and to avoid the loss of communication data.

1) CTS signal
When CTS signal is set to GND, Tc35661 setup the sending data to host CPU. After CTS signal is set to VCC and TC35661 has sending data, TC35661 stops to output sending data to host.

2) RTS signal
When RTS signal is set to GND, host CPU can send data to TC35661. If TC35661 can not arrange to receive the data from host CPU, TC35661 is set RTS signal to VCC.

4.2.4 Procedure of initial control
After to release Reset sequence, TC35661 is set to HCI mode, which is used to set RF IC control parameters. To change from HCI mode to Complete mode, host CPU sends HCI_Set_Mode command in HCI Vendor Specific command.

![Flowchart](image-url)

Bluetooth complete mode. TCU command can be used
4.2.5 Command and response for initialization

After Power on, or HW Reset, the TC35661 hardware is initialized for 20ms. RTS signal is set to high during the sequence of hardware initialization. After a RTS signal is set to low, or the HW Reset is input and waits for 20ms.

Refer to the following flowchart.
4.2.6 Flow chart of initialization

Flow chart during HCI mode

- **M2_BTL_SET_PATCH**
  - Apply patch file to modify firmware

- **M2_BTL_SET_BAUDRATE**
  - Change UART baudrate. Default value is 115200bps.

- **EEPROM support?**
  - Not supported
  - Supported
    - **M2_BTL_SET_I2C_ENABL**
      - Enable I2C interface
    - **M2_GENERAL_READ_E2PROM**
      - Read contents in EEPROM (BD_ADDR, RF parameter, etc)

- **HCI_WRITE_BD_ADDR**
  - Write BD_ADDR on RAM read from EEPROM

- **HCl_DBUS_WRITE**
  - Set RF parameter read from EEPROM.
    (NOTE) Refer to section 8 [RF parameter adjustment].

- **LOC_WRITE_MEM**
  - Enable external clock for Sleep mode

- **M2_BTL_SET_DEEP_SLEEP**
  - Set following parameters during Sleep mode
    1. 32kHz oscillator drift (ppm) on local device
    2. Jitter drift (us) on local device
    3. Sleep mode interval
    Note: These parameters depend on Vendor

- **to Complete mode**
Flow chart during Complete mode

1. **Set Mode**
2. **TCU_MNG_INIT_REQ**
3. **TCU_MNG_STANDARD_HCI_SET_REQ** (Write Class of Device command)
4. **TCU_MNG_LE_INIT_REQ**
5. **TCU_SPP_SETUP_REQ**
6. **TCU_SPP_CONNECT_REQ**
7. **Make Database**
   - **TCU_MNG_SET_SCAN_REQ** or **TCU_MNG_LE_START_ADVERTISE_REQ**

Change from HCI mode to Complete mode:
TC35661 sets RTS to high for 30ms, and returns response to host CPU. In this time host CPU needs to stand by for 30ms.

Set Local Device Name

Set Class of Device

From HCI mode:

Connection initiator?
- TC35661 initiator
- Mobile phone initiator
4.2.7 Command sequence for Complete mode

scenario1
TC35661 doesn’t send Bluetooth data to a remote device.

TCU XXX REQ
TCU XXX RESP

scenario2
TC35661 sends Bluetooth data to a remote device.

TCU XXX REQ
TCU_ACCEPT/TCU_LE_ACCEPT
TCU XXX EVENT

scenario3
A remote device notifies Bluetooth data to a Host CPU.

TCU XXX EVENT

TC3566
Remot Devic
Hos CP
UART Bluetooth
5 EEPROM control

5.1 EEPROM data format
TC35661 can use an eternal EEPROM via an I2C. BD_ADDR, RF parameter, paired device information and user data can be stored into an EEPROM. Following table shows EEPROM fields.

<table>
<thead>
<tr>
<th>Name</th>
<th>Word Addr</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>System field</td>
<td>0x00-0x01</td>
<td>System field</td>
</tr>
<tr>
<td>Data field</td>
<td>0x02-0x07</td>
<td>BD ADDR</td>
</tr>
<tr>
<td></td>
<td>0x08-0x11</td>
<td>Module basic parameters (*Reserved)</td>
</tr>
<tr>
<td></td>
<td>0x12-0x2D</td>
<td>System field</td>
</tr>
<tr>
<td></td>
<td>0x2E-0x37</td>
<td>RF parameter</td>
</tr>
<tr>
<td></td>
<td>0x38-0x6F</td>
<td>Paired device information</td>
</tr>
<tr>
<td></td>
<td>0x70-0x7F</td>
<td>Host CPU can use freely</td>
</tr>
<tr>
<td>System field</td>
<td>0x80-0xFF</td>
<td>System field</td>
</tr>
<tr>
<td>User field</td>
<td>0x100~</td>
<td>Host CPU can use freely</td>
</tr>
</tbody>
</table>

5.2 EEPROM devices information
The following table shows tested EEPROM in Toshiba.

<table>
<thead>
<tr>
<th>Vender</th>
<th>type</th>
<th>size</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROHM</td>
<td>BR24T01NUX-WTR</td>
<td>1kByte</td>
</tr>
<tr>
<td>Seiko Instruments Inc.</td>
<td>S-24C02CI-18T1U</td>
<td>2kByte</td>
</tr>
<tr>
<td>ATMEL</td>
<td>ATMEL52424C256PU18</td>
<td>32kByte</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>M24C32</td>
<td>4kByte</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>M24C64</td>
<td>8kByte</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>M24256</td>
<td>32kByte</td>
</tr>
</tbody>
</table>

5.3 Control command for data writing
(1) Host CPU enable I2C interface with M2_BTL_SET_I2C_ENABLE command.
(2) Host CPU enable EEPROM write access with
   M2_BTL_E2PROM_WRITE_PROTECTION_ENABLE command
(3) Host CPU writes data with M2_GENERAL_WRITE_E2PROM command
(4) Host CPU read data with M2_GENERAL_READ_E2PROM command

Refer to TC35661_Extention_HCI_Command_XXXX.pdf for more detail.
### 6 Pin Specification

<table>
<thead>
<tr>
<th>Pin</th>
<th>During Reset</th>
<th>After Reset</th>
<th>Function change by command</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0</td>
<td>GPIO</td>
<td>GPIO</td>
<td>RequestWakeUp</td>
</tr>
<tr>
<td></td>
<td>Input(HZ)</td>
<td>Input(HZ)</td>
<td>Input(HZ)</td>
</tr>
<tr>
<td>GPIO1</td>
<td>GPIO</td>
<td>GPIO</td>
<td>Status</td>
</tr>
<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
<td>Output(No Pull)</td>
</tr>
<tr>
<td>GPIO2</td>
<td>GPIO</td>
<td>GPIO</td>
<td>PulseOut2</td>
</tr>
<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
<td>Output(No Pull)</td>
</tr>
<tr>
<td>GPIO3</td>
<td>GPIO</td>
<td>GPIO</td>
<td>PulseOut3</td>
</tr>
<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
<td>Output(No Pull)</td>
</tr>
<tr>
<td>GPIO4</td>
<td>GPIO</td>
<td>GPIO</td>
<td>HostWakeUp</td>
</tr>
<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
<td>Output(No Pull)</td>
</tr>
<tr>
<td>GPIO5</td>
<td>GPIO</td>
<td>GPIO</td>
<td>GPIO</td>
</tr>
<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
</tr>
<tr>
<td>GPIO6</td>
<td>GPIO</td>
<td>UART TX</td>
<td>UART TX</td>
</tr>
<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Output(No Pull)</td>
<td>Output(No Pull)</td>
</tr>
<tr>
<td>GPIO7</td>
<td>GPIO</td>
<td>UART RX</td>
<td>UART RX</td>
</tr>
<tr>
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<td>Input(Pull up)</td>
<td>Input(HZ)</td>
<td>Input(No Pull up)</td>
</tr>
<tr>
<td>GPIO8</td>
<td>GPIO</td>
<td>UART RTS</td>
<td>UART RTS</td>
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<td>Output(No Pull)</td>
<td>Output(No Pull)</td>
</tr>
<tr>
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<td>GPIO</td>
<td>UART CTS</td>
<td>UART CTS</td>
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<td>Input(HZ)</td>
<td>Input(No Pull up)</td>
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<td>GPIO</td>
<td>GPIO</td>
<td>GPIO</td>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<tr>
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<td>GPIO</td>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<tr>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<td></td>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<tr>
<td>GPIO16</td>
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<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
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<tr>
<td>GPIO17</td>
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<td>Input(Pull up)</td>
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<tr>
<td>GPIO18</td>
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<tr>
<td></td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
<td>Input(Pull up)</td>
</tr>
</tbody>
</table>
7 Sleep function

7.1 General description
Sleep function decreases consumption. Host CPU controls the following two methods.
1) GPIO0(RequestWakeUp)
2) UART command

7.2 Condition to enter Sleep mode
1) Change Sleep clock to external one (e.g. 32kHz) with LOC_WRITE_MEM command.
2) Sett Sleep mode with M2_BTL_SET_DEEP_SLEEP command.
3) Bluetooth link is not existed or indicated Sniff mode with TCU_MNG_CONNECTION_STATUS_EVENT.

7.2.1 Setting with M2_BTL_SET_DEEP_SLEEP command
M2_BTL_SET_DEEP_SLEEP command controls sleep clock, drift and jitter.
The jitter and drift are used to sync window length for RF receiving. So when the setting value is smaller than actual value, Sniff link might be disconnected. When the setting value is bigger than actual value, sync window for RF receiving opens widely, as the result consumption is increased.

7.2.2 TCU_MNG_DEEP_SLEEP_REQ command description
This command is used to enter/exit deep sleep mode in complete mode.
After Host sends TCU_MNG_DEEP_SLEEP_REQ(Enable),
Host shall send TCU_MNG_DEEP_SLEEP_REQ(Disable) before sending other commands.
TC35661 enters deep sleep mode after receiving TCU_MNG_DEEP_SLEEP_REQ(Enable).
Then TC35661 recognizes all commands as TCU_MNG_DEEP_SLEEP_REQ(Disable) command during deep sleep mode.
7.3 Function in Sleep mode

7.3.1 Sleep mode control by GPIO

Host CPU controls GPIO0. TC35661 notify sleep status with GPIO1. M2_BTL_SET_DEEP_SLEEP command (Deep-sleep instructions/ Set Notify specific interface) sets method. Select Bit0: GPIO (0=No notification / 1=Notification).

GPIO0=H: Sleep is not available.
GPIO0=L: Sleep is available.
GPIO1=H: Sleep mode. Host can not send UART command.
GPIO1=L: Active mode. Host can send UART command.

These following figures show control Sleep mode by using GPIOs.

**During no Bluetooth link**

<table>
<thead>
<tr>
<th>GPIO0(RequestWakeUp) MCU -&gt; TC35661</th>
<th>Low level (Request Sleep mode) Host CPU cannot transmit UART commands.</th>
<th>Status is changed from Active mode to Sleep mode after 4ms.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO1(Status) TC35661 -&gt; MCU Low level</td>
<td>High level (Sleep mode is not available) Host CPU can transmit UART commands.</td>
<td>Status is changed from Sleep mode to Active mode after 1ms.</td>
</tr>
</tbody>
</table>

**During no Bluetooth link / Running Scan mode**

<table>
<thead>
<tr>
<th>GPIO0(RequestWakeUp) MCU -&gt; TC35661</th>
<th>Low level (Sleep mode) Host CPU cannot transmit UART commands.</th>
<th>Shift to Active mode during Scan Window</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO1(Status) TC35661 -&gt; MCU High level (Sleep mode)</td>
<td>Scan Interval</td>
<td></td>
</tr>
</tbody>
</table>
7.3.2 Sleep mode procedure by GPIO

1) Send LOC_WRITE_MEM command during HCI mode to use external sleep clock.
2) Send M2_BTL_SET_DEEP_SLEEP command during HCI mode.
   This command can set to Sleep mode and change Sleep clock jitter and drift with this command.
3) Input high to GPIO0 (No Sleep mode).
4) Connect SPP.
5) Set to sniff mode with TCU_MNG_SNIFF_MODE_CONTROL_REQ command.
6) Input GPIO0 to low to enter Sleep mode.
7.3.3 Sleep mode control by UART command

M2_BTL_SET_DEEP_SLEEP command (Deep-sleep instructions/Set Notify specific interface) sets control method. Select Bit1: UART (0=No notification / 1=Notification).

When UART is selected, TCU_MNG_DEEP_SLEEP_REQ (TC35661APL_MNG_E_XXXX.pdf) controls sleep mode. SPP firmware does not support USB.

The figure shows relationship between TCU_MNG_DEEP_SLEEP_REQ/parameter and GPIO1 notify.

**During no Bluetooth link**

GPIO0 (RequestWakeUp)

- Host CPU sends TCU_MNG_DEEP_SLEEP_REQ(Enable).
- Host CPU sends TCU_MNG_DEEP_SLEEP_REQ(Disable).

GPIO1(Status) TC35661->MCU Low level.

**During Bluetooth link / Running Scan mode**

- Host CPU sends TCU_MNG_DEEP_SLEEP_REQ(Enable).
- Host CPU sends TCU_MNG_DEEP_SLEEP_REQ(Disable).
- Host CPU can transmit UART data when GPIO1 is low level.
- When Host CPU sends UART data during this timing, the data cannot be sent during this sniff attempt. TC35661 sends the data on the next Sniff Attempt.

7.3.4 Sleep mode procedure by UART command

1) Send LOC_WRITE_MEM command during HCI mode to use external sleep clock.
2) Send M2_BTL_SET_DEEP_SLEEP command during HCI mode.
   This command can set to Sleep mode and change Sleep clock jitter and drift with this command.
3) Connect SPP.
4) Set to sniff mode with TCU_MNG_SNIFF_MODE_CONTROL_REQ command.
5) Send TCU_MNG_DEPTH_SLEEP_REQ command to set to Sleep mode.
7.4 HostWakeUp signal

7.4.1 HostWakeUp Description
TCU_VEN_SET_HOST_WAKEUP_NOTIFICATION_REQ command enables HostWakeUp signal with GPIO4. HostWakeUp signal wakes up host CPU from Sleep mode. Both host CPU and TC35661 can be entered Sleep mode to reduce the system power consumption.

7.4.2 The example of sequence using HostWakeUp signal
1) Send TCU_VEN_SET_HOST_WAKEUP_NOTIFICATION_REQ command (Enable) from host CPU.
2) TC35661 starts to control a HostWakeUp signal simultaneously with TCU_VEN_SET_HOST_WAKEUP_NOTIFICATION_RESP from host CPU.
3) Host CPU needs to turn a BT_CTS to high before sleep mode.
4) TC35661 is waked up by receiving the data from remote device.
5) TC35661 outputs a HostWakeUp signal to host CPU.
6) Host CPU shifts to Active mode by receiving the HostWakeUp signal.
7) After host CPU is weaked up from sleep mode, host CPU turns BT_CTS signal to low. Then TC35661 generates data.

![Diagram showing sequence of events involving HostWakeUp signal](image-url)
8 RF parameter adjustment

The X'tal frequency parameter can be adjusted by DBUS_WRITE_MEM command.
The default value is 0x0100.

8.1 RF parameters adjustment method

HCI_DBUS_WRITE command line is 03 fc 05 00 c2 a6 xx xx, and xx xx is value to set X'tal frequency.
The 0xa6 means that the most significant 3bits are the device address, and the least significant 5bits are
the RF parameter address.

HCI_DBUS_READ command reads RF parameters. This command line is 03 fc 03 00 c3 a6.

Refer to TC35661_Extension_HCI_Command_E_XXXX.pdf for more detail.
X'tal frequency parameter is 1-2kHz per 1step.
Refer to Datasheet in order to get some exact information.

(Note)
Evaluate frequency after the parameter changes in each environment.

8.2 Characteristic improvement

ROM501 needs additional command to improve RF characteristics.
Script file name is tc35661v5_RM501_130725LEdual_power_con_enable.txt
Command line is as follows.
When this command line is not implemented, RF for low energy characteristic might be not enough.

ExCh3- Op=0xfc03  len=0x05  mesgID=0xc2(LOC_DBUS_WRITE)  addr=0xae(dev:0x5,reg:0x0e)
value=0xcd18
L:(CMD) 01 03 fc 05 00 c2 ae 18 cd
B:(EVT) 04 0f 04 00 04 03 fc
B:(EVT) 04 ff 04 03 00 c2 00
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 ee 00 d9
ExCh3- Op=0xfc03  len=0x05  mesgID=0xc2(LOC_DBUS_WRITE)  addr=0xee(dev:0x7,reg:0x0e)
value=0xd900
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 a4 a4
ExCh3- Op=0xfc03  len=0x05  mesgID=0xc2(LOC_DBUS_WRITE)  addr=0xfa(dev:0x7,reg:0x1a) value=0xa4a4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 81 f3 c7
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x81(dev:0x4,reg:0x01) value=0xc7f3
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MsgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 63 f4 04
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x63(dev:0x3,reg:0x03) value=0x04f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MsgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 83 00 e6
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x83(dev:0x4,reg:0x03) value=0xe600
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MsgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 64 af 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x64(dev:0x3,reg:0x04) value=0x00af
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MsgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 84 ff 80
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x84(dev:0x4,reg:0x04) value=0x80ff
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MsgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 65 b0 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x65(dev:0x3,reg:0x05) value=0x00b0
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MsgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 85 1b 60
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x85(dev:0x4,reg:0x05)
value=0x601b
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 66 ed 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x66(dev:0x3,reg:0x06)
value=0x00ed
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 86 6e 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x86(dev:0x4,reg:0x06)
value=0x006e
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 67 ea 0e
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x67(dev:0x3,reg:0x07)
value=0x0eea
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 87 80 80
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x87(dev:0x4,reg:0x07)
value=0x8080
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 68 f4 49
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x68(dev:0x3,reg:0x08) value=0x49f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:\(\text{CMD}\) 01 03 fc 05 00 c2 88 00 ee
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x88(dev:0x4,reg:0x08)
value=0xee00
B:\(\text{EVT}\) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:\(\text{EVT}\) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:\(\text{CMD}\) 01 03 fc 05 00 c2 69 f4 27
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x69(dev:0x3,reg:0x09) value=0x27f4
B:\(\text{EVT}\) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:\(\text{EVT}\) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:\(\text{CMD}\) 01 03 fc 05 00 c2 89 00 fe
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x89(dev:0x4,reg:0x09) value=0xfe00
B:\(\text{EVT}\) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:\(\text{EVT}\) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:\(\text{CMD}\) 01 03 fc 05 00 c2 6a 00 ff
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x6a(dev:0x3,reg:0x0a) value=0xff00
B:\(\text{EVT}\) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:\(\text{EVT}\) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:\(\text{CMD}\) 01 03 fc 05 00 c2 8a 00 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x8a(dev:0x4,reg:0x0a)
value=0x0000
B:\(\text{EVT}\) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:\(\text{EVT}\) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:\(\text{CMD}\) 01 03 fc 05 00 c2 6b ea 09
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x6b(dev:0x3,reg:0x0b)
value=0x09ea
B:\(\text{EVT}\) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:\(\text{EVT}\) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:\(\text{CMD}\) 01 03 fc 05 00 c2 8b 80 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x8b(dev:0x4,reg:0x0b)
value=0x0080

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B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 6c f4 01
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6c(dev:0x3,reg:0x0c) value=0x01f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8c 00 80
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8c(dev:0x4,reg:0x0c) value=0x0800
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6d e2 01
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6d(dev:0x3,reg:0x0d) value=0x01e2
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8d 08 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8d(dev:0x4,reg:0x0d) value=0x0008
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6e a4 01
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6e(dev:0x3,reg:0x0e) value=0x01a4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8e 80 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8e(dev:0x4,reg:0x0e) value=0x0080
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 6f 00 ff
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6f(dev:0x3,reg:0x0f) value=0xff00
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) msgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8f 00 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8f(dev:0x4,reg:0x0f) value=0x0000
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) msgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 a0 21 10
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0xa0(dev:0x5,reg:0x00)
value=0x1021
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) msgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 81 d3 c7
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x81(dev:0x4,reg:0x01)
value=0xc7d3
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) msgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 82 a8 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0xa8(dev:0x5,reg:0x02)
value=0x00a8
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) msgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 63 f4 04
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x63(dev:0x3,reg:0x03)
value=0x04f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) msgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 83 00 e2
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x83(dev:0x4,reg:0x03) value=0xe200
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 64 af 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x64(dev:0x3,reg:0x04) value=0x00af
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 84 f8 80
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x84(dev:0x4,reg:0x04) value=0x80f8
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 65 b0 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x65(dev:0x3,reg:0x05) value=0x00b0
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 85 18 60
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x85(dev:0x4,reg:0x05) value=0x6018
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 66 ed 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x66(dev:0x3,reg:0x06) value=0x00ed
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 86 6e 70
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x86(dev:0x4,reg:0x06)
value=0x706e
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 67 ea 0e
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x67(dev:0x3,reg:0x07)
value=0x0eea
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 87 80 80
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x87(dev:0x4,reg:0x08)
value=0x8080
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 68 f4 14
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x68(dev:0x3,reg:0x08)
value=0x14f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 88 00 e6
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x88(dev:0x4,reg:0x08)
value=0xe600
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 69 f4 04
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x69(dev:0x3,reg:0x09)
value=0x04f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 89 00 fe
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x89(dev:0x4,reg:0x09) value=0xfe00
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6a 00 ff
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6a(dev:0x3,reg:0x0a) value=0xff00
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8a 00 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8a(dev:0x4,reg:0x0a) value=0x0000
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6b ea 02
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6b(dev:0x3,reg:0x0b) value=0x02ea
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8b 80 00
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8b(dev:0x4,reg:0x0b) value=0x8080
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6c f4 01
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x6c(dev:0x3,reg:0x0c) value=0x01f4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8c 00 80
ExCh3- Op=0xfc03 len=0x05 msgID=0xc2(LOC_DBUS_WRITE) addr=0x8c(dev:0x4,reg:0x0c) value=0x8000
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 03 fc 05 00 c2 6d e2 01
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x6d(dev:0x3,reg:0x0d) value=0x01e2
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8d 08 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x8d(dev:0x4,reg:0x0d) value=0x008
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6e a4 01
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x6e(dev:0x3,reg:0x0e) value=0x01a4
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8e 80 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x8e(dev:0x4,reg:0x0e) value=0x0080
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 6f 00 ff
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x6f(dev:0x3,reg:0x0f) value=0xff00
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 8f 00 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0x8f(dev:0x4,reg:0x0f) value=0x0000
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)

L:(CMD) 01 03 fc 05 00 c2 a0 21 00
ExCh3- Op=0xfc03 len=0x05 mesgID=0xc2(LOC_DBUS_WRITE) addr=0xa0(dev:0x5,reg:0x00)
value=0x0021
B:(EVT) 04 0f 04 00 04 03 fc
Command_Status- st=0x00(SUCCESS) NHCP=0x04 Op=0xfc03(ExCh3)
B:(EVT) 04 ff 04 03 00 c2 00
Ext_Event-ExCh3(LCI) MesgID=0xc2(LOC_DBUS_WRITE) st=0x00(LOC_OK)
L:(CMD) 01 08 fc 2f 00 a0 00 00 00 14 55 ff 10 25 03 9c ad 09 00 e0 7b 00 28 01 d0 02 21 38 e0 bb f7 ab fe 4a e1 01 d0 e5 f7 7e ff 01 2e 00 d0 00 27 20 7c 04 28
ExCh8- Op=0xfc08 len=0x2f ExOp=0xa0(M2_Set) Initiator=0x04(Host) Acceptor=0x01(BT_Core_lower)
InformationID=0x55(PATCH_SWAP_BASE)
- Result=0xff(Result_Reserved) DataType=0x10(Bytes) DataLength=0x25
Data=0x039cad0900e7b002801d0022138e0bbf7abfe4ae101d0ef77eff012e00d00027207c0428
B:(EVT) 04 ff 0a 00 00 00 00 14 56 ff 10 e4 00 6b 05 00 26 4a 01 04 20 80 20 34 00 23 02 1c 9a 43 0a 80 17
4a 03 23 5b 04 5a 62 60 32 da 62 16 4a 14 4d 5a 66 15 4a 17 4c 9a 66 15 4a 5a 67 da 1d f9 32 9d 62 54 62 08 34 d4 62 95 62 13 4a 12 4c 54 62 13 4c 94 62 13 4c d4 62 1b 68 12 4a 93 42 0d d1 08 80 30 bc 70 47 20 02 06 00 c0 08 06 00 be 2f 00 00 60 03 06 00 60 06 00 a0 02 06 00 0b 20 00 20 20 18 20 07 a0 01 21 00 a0 1d 21 0c a0 01 21 0f 20 00 20 01 20 01 20 40 01 06 00 00 20 1d 03 20 01 20 0f 00 00
ExCh8- Op=0xfc08 len=0xee ExOp=0xa0(M2_Set) Initiator=0x04(Host) Acceptor=0x01(BT_Core_lower)
InformationID=0x56(PATCH_SWAP_PROG_WRITE)
- Result=0xff(Result_Reserved) DataLength=0x2e
Data=0x006b0500264a052030b4108026482549882ff20c882c88a007fcd1012080038882488b0009000108 2
101435183ff21ff3191831d4c0022a280ff23e4333e800c2404431a488481c1818282c382194908880123021c9a 430a80174a03235b045a626032da62164a144d5a6615a4a174c9a6615a5a67da1df329d6254620834d46295 6
2134a124c5462134c9462134cd4621b68124a9342fdd1088030bc704720020600c0080600be2f00060030600600b0600a00026000b200020020182007a0012100a01210ca001210f2000201200120401006000201d20 0
3200120ff0000
B:(EVT) 04 ff 0a 08 00 a0 00 00 00 14 56 00 00
Ext_Event-ExCh8(Toshiba) M2_Set Initiator=0x04(Host) Acceptor=0x01(BT_Core_lower)
InformationID=0x56(PATCH_SWAP_PROG_WRITE)
- Result=0x00(OK) DataLength=0x00
Data=0x006b0500264a052030b4108026482549882ff20c882c88a007fcd1012080038882488b0009000108 2
101435183ff21ff3191831d4c0022a280ff23e4333e800c2404431a488481c1818282c382194908880123021c9a 430a80174a03235b045a626032da62164a144d5a6615a4a174c9a6615a5a67da1df329d6254620834d46295 6
2134a124c5462134c9462134cd4621b68124a9342fdd1088030bc704720020600c0080600be2f00060030600600b0600a00026000b200020020182007a0012100a01210ca001210f2000201200120401006000201d20 0
3200120ff0000
B:(EVT) 04 ff 0a 08 00 a0 00 00 00 14 56 00 00
Ext_Event-ExCh8(Toshiba) M2_Set Initiator=0x04(Host) Acceptor=0x01(BT_Core_lower)
InformationID=0x57(PATCH_CONTROL)
- Result=0xff(Result Reserved) DataLength=0x02(Uint16) Data=0x0103
B:(EVT) 04 ff 0a 08 00 a0 00 00 00 14 56 00 00
Ext_Event-ExCh8(Toshiba) M2_Set Initiator=0x04(Host) Acceptor=0x01(BT_Core_lower)
InformationID=0x57(PATCH_CONTROL)
- Result=0x00(OK) DataLength=0x00

L:(CMD) 01 08 fc 09 00 a0 00 00 00 14 01 ff 00  
ExCh8- Op=0xfc08 len=0x09 ExOp=0xa0(M2_Set) Initiator=0x04(Host) Accepter=0x01(BT_Core_lower)  
InformationID=0x01(TRACE_START)  
    - Result=0xff(Result_Reserved) DataType=0x00(Data_None)  
B:(EVT) 04 ff 0a 08 00 a0 00 00 00 14 01 02 00  
Ext_Event-ExCh8(Toshiba) M2_Set Initiator=0x04(Host) Accepter=0x01(BT_Core_lower)  
InformationID=0x01(TRACE_START)  
    - Result=0x02(Unknown_Data_Type) DataType=0x00(Data_None)
9 Control GPIOs output

9.1 GPIOs output control command

GPIOs are set to input ports (Internal PullUp) after resets. Only GPIO0 is no internal register. TCU_VEN_SET_GPIO_WRITE_REQ command enables GPIOs to output ports. This command is available on both active and Sniff mode.

The following figure shows the sequence.

![Sequence Diagram]

- It is possible to turn to High/Low during Sniff mode.
- Status of GPIOs is internal PullUp immediately after power.
9.2 GPIOs pulse mode control command

TCU_VEN_SET_GPIO_PULSE_REQ command repeats GPIO2 and GPIO3 to high and low output periodically.

This command is used for LEDs blink.

GPIOs blink is kept during Sleep mode.

The following figure shows the sequence.

End of document